What is claimed is:

1. A driving circuit for switches of direct current fan motor comprising:

a plurality of switches driven by a first pulse width modulation (PWM) signal and a second PWM signal;

a first control circuit electrically connected with at least one switch driven by the first PWM signal, and driven by a third PWM signal; and

a second control circuit electrically connected with at least one switch driven by the second PWM signal, and driven by a fourth PWM signal;

wherein, when the first PWM signal is at a low level, the switches driven by the first PWM signal are in an OFF state, and the third PWM signal drives the first control circuit and locks the switches driven by the first PWM signal to an OFF state; and when the second PWM is at a low level, the switches driven by the second PWM are in an OFF state, and the fourth PWM signal drives the second control circuit and locks the switches driven by the second PWM signal to an OFF state.

2. The driving circuit for switches of direct current fan motor as described in claim 1, wherein the third PWM signal is the first PWM signal, and the fourth PWM signal is the second PWM signal.

3. The driving circuit for switches of direct current fan motor as described in claim 1, wherein the third PWM signal is the second PWM signal, and the fourth PWM signal is the first PWM signal.

4. The driving circuit for switches of direct current fan motor as described in claim 1, wherein the switches have n-channel enhancement-mode metal-oxide semiconductor field-effect transistors (MOSFET) and p-channel enhancement-mode MOSFET.

5. The driving circuit for switches of direct current fan motor as described in claim 1, wherein the first control circuit and the second control circuit have an n-channel enhancement-mode MOSFET, respectively.

6. The driving circuit for switches of direct current fan motor as described in claim 1, further comprising:

a third control circuit electrically connected with switches driven by the first PWM signal, and driven by a fifth PWM signal; and

a fourth control circuit electrically connected with switches driven by the second PWM signal, and driven by a sixth PWM signal;

wherein, when the first PWM signal and the second PWM signal are simultaneously at a low level, the fifth PWM signal drives the third control circuit and locks the switch driven by the first PWM signal to an OFF state, and the sixth PWM signal drives the fourth control circuit and locks the switch driven by the second PWM signal to an OFF state.

7. The driving circuit for switches of direct current fan motor as described in claim 6, wherein the fifth PWM signal is identical to the sixth PWM signal, and is an output signal of a NOR logic gate receiving and processing the first PWM signal and the second PWM signal.

8. The driving circuit for switches of direct current fan motor as described in claim 6, wherein the third control circuit and the fourth control circuit have an n-channel enhancement-mode MOSFET, respectively.

9. A driving circuit for switches of direct current fan motor comprising:

two first switches connected with the direct current fan motor in a bridge manner, and driven by a first PWM signal and a second PWM signal, respectively;

a first control circuit electrically connected with the first switch driven by the first PWM signal, and driven by the first PWM signal and a first applied voltage; and

a second control circuit electrically connected with the first switch driven by the second PWM signal, and driven by the second PWM signal and a second applied voltage;

wherein, when the first PWM signal is at a low level, the first switch driven by the first PWM signal is in an OFF state; and when the second PWM signal is at a low level, the first switch driven by the second PWM signal is in an OFF state.

10. The driving circuit for switches of direct current fan motor as described in claim 9, wherein the first and second control circuits have a second switch, respectively; when the first PWM signal and the second PWM signal are simultaneously at a low level, the second switch of the first control circuit is in an ON state and forms a loop with the first switch driven by the first PWM signal, and the second switch of the second control circuit is in an ON state and forms a loop with the first switch driven by the second PWM signal.

11. The driving circuit for switches of direct current fan motor as described in claim 9,

wherein the first switches are n-channel enhancement-mode MOSFET.

12. The driving circuit for switches of direct current fan motor as described in claim 10, wherein the second switches are n-channel enhancement-mode MOSFET, and when the first PWM signal and the second PWM signal are simultaneously at a low level, potential difference between a gate and a source of the first switches are zero.

13. The driving circuit for switches of direct current fan motor as described in claim 9, further comprising two second switches connected with the direct current fan motor and the first switches in a bridge manner, and driven by the first PWM signal and the second PWM signal, respectively.

14. The driving circuit for switches of direct current fan motor as described in claim 13, wherein the second switches are p-channel enhancement-mode MOSFET.

15. A driving circuit for switches of direct current fan motor comprising:

two first switches electrically connected with the direct current fan motor in a bridge manner, and driven by a first PWM signal and a second PWM signal, respectively;

a first control circuit electrically connected with the first switch driven by the first PWM signal, and driven by the second PWM signal;

a second control circuit electrically connected with the first switch driven by the second PWM signal, and driven by the first PWM signal;

a NOR logic gate for receiving the first PWM signal and the second PWM signal, and

outputting a third PWM signal;

a third control circuit electrically connected with the first switch driven by the first PWM signal, and driven by the third PWM signal; and

a fourth control circuit electrically with the first switch driven by the second PWM signal, and driven by the third PWM signal;

wherein, when the first PWM signal is at a low level, the first switch driven by the first PWM signal is in an OFF state; and when the second PWM signal is at a low level, the first switch driven by the second PWM signal is in an OFF state.

16. The driving circuit for switches of direct current fan motor as described in claim 15, wherein the third control circuit and the fourth control circuit have a second switch, respectively, and when the first PWM signal and the second PWM signal are simultaneously at a low level, the second switches are in an ON state and forms a loop with the first switches.

17. The driving circuit for switches of direct current fan motor as described in claim 15, wherein the first control circuit and the second control circuit have a third switch, respectively, and when the first PWM signal is at a low level and the second PWM signal is at a high level, the third switch of the first control circuit is in an ON state and forms a loop with the first switch driven by the first control circuit; and when the second PWM signal is at a low level and the first PWM signal is at a high level, the third switch of the second control circuit is in an ON state and forms a loop with the first switch driven by the second PWM signal.

18. The driving circuit for switches of direct current fan motor as described in claim 15,

wherein the first switches are n-channel enhancement-mode MOSFET.

19. The driving circuit for switches of direct current fan motor as described in claim 16, wherein the second switches are n-channel enhancement-mode MOSFET, and when the first PWM signal and the second PWM signal are simultaneously at a low level, potential difference between gates and sources of the first switches are zero.

20. The driving circuit for switches of direct current fan motor as described in claim 19, wherein the third switches are n-channel enhancement-mode MOSFET, and when the first PWM signal is at a low level and the second PWM signal is at a high level, potential difference between the gate and source of the first switches driven by the first PWM signal are zero; and when the second PWM signal is at a low level and the first PWM signal is at a high level, potential difference between the gate and source of the first switches driven by the second PWM signal are zero.

21. The driving circuit for switches of direct current fan motor as described in claim 15, further comprising two second switches electrically connected with the direct current fan motor and the first switches in a bridge manner, and driven by the first PWM signal and the second PWM signal, respectively.

22. The driving circuit for switches of direct current fan motor as described in claim 21, wherein the second switches are p-channel enhancement-mode MOSFET.